an electrical connection between each of said passive components and at least a portion of said second series of resistive/conductive patterns on said outer surface of said unitary device body.

20. The multi-layer electrical device of claim 19, wherein said first and second layer are made of FR4.

21. The multi-layer electrical device of claim 20, wherein said device is a printed circuit board.

22. The multi-layer electrical device of claim 19, wherein said first and second layers are made of a non-conductive ceramic.

23. (Amended) The multi-layer electrical device of claim 22, wherein said device is an integrated passive component.

24. The multi-layer electrical device of claim 19, wherein said passive components comprise any combination of resistors, capacitors, varistors, and thermistors.

25. (Amended) A multi-layer electronic device comprising:

a plurality of first device layers, each such layer having a first series of resistive/conductive patterns thereon and a plurality of via drilled therethrough;

a plurality of second device layers, each such layer having a plurality of via drilled therethrough;

a unitary device body formed by the bonded union of an interleaved stack of said plurality of first and said second device layers, wherein each of said via correspond to a respective portion of the resistive/conductive patterns on the underlying device layer and wherein one of said second device layers forms the uppermost device layer and the lowermost device layer is one of said first device layers;

a second series of resistive/conductive patterns on an outer layer of said uppermost device layer;

a plurality of terminations on said unitary body for electrical connection between other electronic devices and various of the resistive/conductive patterns throughout said unitary device body;

individual passive components with respective first and second opposing terminations, wherein each individual passive component is vertically mounted into a selected of said plurality of via and wherein one of said first and second opposing terminations are electrically connected to a portion of said underlying first device layer's first series of resistive/conductive patterns;

multiple portions of a non-conductive material respectively substantially filling the space between each of said individual passive components and the surrounding via, wherein said non-conductive material partially encases each said individual passive component to hold it in place while leaving one of said first and second opposing electrical terminations exposed and prevents shorting between respective first and second opposing electrical terminations; and

an electrical connection between each of said passive components and at least a portion of said overlying first device layer's first series of resistive/conductive patterns through a corresponding one of said first device layer's plurality of via.

RESPONSE

SUMMARY:

The subject application sets forth original claims 19-25, of which claims 19 and 25 are independent claims. The title of the invention stands objected to for allegedly lacking appropriate description. Certain aspects of the drawings stand objected to as discussed in further detail below. Claim 23 stands objected to for a dependency informality. Claim 25 stands initially rejected under 35 U.S.C. §102(b) as being allegedly anticipated by U.S. Patent No. 4,800,459 (Takagi et al.). Claims 19 and 22-24 stand initially rejected under 35 U.S.C. §103(a) as allegedly obvious over U.S. Patent No. 4,800,459 (Takagi et al.) in view of U.S. Patent Application Publication No. 2002/0145203 (Adae-Amoakoh). Claims 20 and 21 stand initially rejected under 35 U.S.C. §103(a) as allegedly obvious over U.S. Patent No. 4,800,459 (Takagi et al.) in

view of U.S. Patent Application Publication No. 2002/0145203 (Adae-Amoakoh) and U.S. Patent N. 6,471,525 (Fan et al.).

OBJECTION TO THE SPECIFICATION:

Per the Examiner's request, the title of the invention has been amended to provide a more descriptive title that is indicative of the invention to which the claims are directed. As such, the title of the invention as presently amended reads "MULTILAYER ELECTRONIC DEVICES WITH VIA COMPONENTS." Such amendment does not add any new matter to the specification.

OBJECTION TO THE DRAWINGS:

Objections were made with regard to Figures 1 and 2, alleging that such figures should be designated with an appropriate legend since only that which is old is illustrated. As such, Figures 1 and 2 have been amended herein to indicated both such figures as "Prior Art." In accordance with 37 CFR §1.121(d), a separate sheet depicting in red ink such proposed changes to Figures 1 and 2, is submitted in Appendix B for approval by the Examiner.

The drawings stand objected to under 37 C.F.R. §1.84(p)(4) because reference numeral 51 as mentioned in the specification is not illustrated in the drawings. Also, reference numerals 52 and 54 are shown in Figure 5 but not mentioned in the specification. As such, Figure 5 is presently amended to modify previous reference numerals 52, 54 and 66 to numerals 22, 24 and 51 respectively. A separate sheet depicting in red ink such proposed changes to Figure 5 is submitted in Appendix B for approval by the Examiner.

The drawings are objected to for failing to comply with 37 C.F.R. 1.84(p)(4) because reference character "114" was used to designate both intermediate components and passive components (pg. 14, lines 9-11) and because reference character "160" was used to designate both electrical connections and terminations (pg. 15, lines 10-11). In response, the first full paragraph on page 14 is amended herein to more appropriately indicate 114 as referring to passive components. Also, the first full paragraph on page 15 is amended herein to provide consistent correlation between

reference numeral 160 and "terminations," although Applicant submits that a termination is merely a specific kind of electrical connection, and thus such terminology may be interchangeable in certain instances. Such responsive amendments are submitted merely to correct inadvertent typographical errors and do not add any new matter to the subject application.

A still further objection to the drawings concerned Figure 13 for illustrating reference numeral 118, wherein such reference numeral was lacking corresponding description in the specification. As such, the first full paragraph of page 16 has been amended to indicate that the previously referred to conductor or solder paste that can be used to fill in the remaining portion of via 148 corresponds to reference numeral 118. Such amendment to the specification does not add any new matter to the present application. Additional proposed modification to Figure 13 is presented in Appendix B to correct inadvertent transposition of reference numerals 118 and 164.

OBJECTION TO CLAIM 23:

Claim 23 stands objected to for dependency informalities because as originally set forth claim 23 depends from itself. As such, claim 23 is amended herein to correct an inadvertent typographical error, where dependence on claim 22 was originally intended.

REJECTION OF ORIGINAL CLAIM 25 (35 U.S.C. §102(b)):

Claim 25 stands initially rejected under 35 U.S.C. §102(b) as being allegedly anticipated by U.S. Patent No. 4,800,459 (Takagi et al.). In view of the remarks presented hereafter, Applicant respectfully traverses such alleged anticipation.

As presently amended, claim 25 is set forth to include an additional feature, namely multiple portions of a non-conductive material respectively substantially filling the space between each of said individual passive components and the surrounding via. Such feature as presently set forth in claim 25 is not disclosed in Takagi et al., and thus such reference cannot by law serve to anticipate claim 25.

The provision of such portions of non-conductive material to partially encompass each passive component in the multilayer electronic device of claim 25 effects several

simultaneous functions. A first such function corresponds to more securely positioning each individual passive component in place in its selected via location. A further function corresponds to preventing shorts between respective first and second opposing electrical terminations of each passive component. By sealing the passive components in place, the nonconductive material prevents any solder from running down the sides of the vias and shorting out the component or interfering with other electrical connections in the multilayer electronic device.

Takagi et al. does not disclose such additional non-conductive material for partially encompassing each passive component. In contrast, each layer 4-6 is formed with through-holes that are specifically designed such that the formation of respect chip-like components may be positioned and effectively formed therein. More particularly, for example, when it is desired to have two capacitors 26 and 27 and one resistor 28 as in the example illustrated in Figure 1, respective spaces 23-25 are formed to specifically accommodate such preselected components. (Col. 1, lines 11-50).

The multilayer electronic device set forth in present claim 25 provides advantages to the technology disclosed in Takagi et al. The non-conductive filler material of claim 25 simultaneously secures the respective passive devices and also prevents undesirable electrical shorting. No such provision is disclosed in Takagi et al. Furthermore, by providing vias that are not necessarily designed for respective specific components, a great amount of design versatility is afforded. As such, a plurality of different types and sizes of passive components can be positioned into each via and afterwards at least partially surrounded by non-conductive filler material. This eliminates the time-consuming and often costly need to form each via to suit particular device dimensions.

Since all of the elements set forth in claim 25 as presently amended are not disclosed in Takagi et al., Applicant respectfully submits that present claim 25 is in condition for allowance and acknowledgement of the same is earnestly solicited.

REJECTION OF ORIGINAL CLAIMS 19 AND 22-24 (35 U.S.C. §103(a)):

Claims 19 and 22-24 stand initially rejected under 35 U.S.C. §103(a) as allegedly obvious over U.S. Patent No. 4,800,459 (Takagi et al.) in view of U.S. Patent

Application Publication No. 2002/0145203 (Adae-Amoakoh). In view of the remarks presented hereafter, Applicant respectfully traverses such alleged obviousness.

As presently amended, claim 19 is set forth to include an additional feature, namely multiple portions of a non-conductive material respectively substantially filling the space between each of said individual passive components and the surrounding via. Such feature as presently set forth in claim 19 is not disclosed in Takagi et al. or in Adae-Amoakoh and thus Applicants respectfully traverse such allegation of obviousness.

The provision of such portions of non-conductive material to partially encompass each passive component in the multilayer electrical device of claim 19 provides several simultaneous functions. A first such function corresponds to more securely positioning each individual passive component in place in its selected via location. A further function corresponds to preventing shorts between respective first and second opposing electrical terminations of each passive component. By sealing the passive components in place, the nonconductive material prevents any solder from running down the sides of the vias and shorting out the component or interfering with other electrical connections in the multilayer electronic device.

Takagi et al. does not disclose such additional non-conductive material for partially encompassing each passive component. In contrast, each layer 4-6 is formed with through-holes that are specifically designed such that the formation of respect chip-like components may be positioned and effectively formed therein. More particularly, for example, when it is desired to have two capacitors 26 and 27 and one resistor 28 as in the example illustrated in Figure 1, respective spaces 23-25 are formed to specifically accommodate such preselected components. (Col. 1, lines 11-50).

The multilayer electronic device set forth in present claim 19 provides advantages to the technology disclosed in Takagi et al. and Adae-Amoakoh. The non-conductive filler material of claim 19 simultaneously secures the respective passive devices and also prevents undesirable electrical shorting. No such provision is disclosed in Takagi et al. or Adae-Amoakoh. Furthermore, by providing vias that are not necessarily designed for respective specific components, a great amount of design versatility is afforded. As such, a plurality of different types and sizes of passive

components can be positioned into each via and afterwards at least partially surrounded by non-conductive filler material. This eliminates the time-consuming and often costly need to form each via to suit particular device dimensions.

Since all of the elements set forth in claim 19 as presently amended are not disclosed singularly or in combination of the Takagi et al. and Adae-Amoakoh references, Applicant respectfully submits that present claim 19 is in condition for allowance and acknowledgement of the same is earnestly solicited. Since claims 22-24 depend either directly or indirectly from otherwise allowable claim 19 and further limit same, claims 22-24 should also be allowable, and acknowledgement of the same is earnestly solicited.

REJECTION OF ORIGINAL CLAIMS 20 AND 21 (35 U.S.C. §103(a)):

Claims 20 and 21 stand initially rejected under 35 U.S.C. §103(a) as allegedly obvious over U.S. Patent No. 4,800,459 (Takagi et al.) in view of U.S. Patent Application Publication No. 2002/0145203 (Adae-Amoakoh) and U.S. Patent N. 6,471,525 (Fan et al.). In view of the remarks presented hereafter, such alleged obviousness is respectfully traversed.

Based on the previous remarks concerning independent claim 19, Applicant submits that claim 19 as presently amended is in complete condition for a notice of allowance. Since claims 20 and 21 variously depend from such otherwise allowable claim and further limit same, claims 20-21 should also be allowable, and acknowledgement of the same is earnestly solicited.

CONCLUSION:

Inasmuch as all outstanding issues have been addressed it is respectfully submitted that the present application, including claims 19-25, is in complete condition for issuance of a formal Notice of Allowance, and action to such effect is earnestly solicited. The Examiner is invited to telephone the undersigned at his convenience should only minor issues remain after consideration of this Amendment and Response in order to permit early resolution of the same.

Respectfully submitted,

DORITY & MANNING,
Attorneys at Law, P.A.

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Date

Jennifer L. van der Horst
Jennifer L. van der Horst, Patent Agent
Registration No.: 52,312
Richard M. Moose, Esquire
Registration No.: 31,226

Post Office Box 1449
Greenville, South Carolina 29602-1449
Telephone: (864) 271-1592
Facsimile: (864) 233-7342